HELSINGIN YLIOPISTO
HELSINGFORS UNIVERSITET
UNIVERSITY OF HELSINKI

581365 Tietokoneen rakenne
Computer Organization II

Spring 2010

Tiina Niklander

Matemaattis-luonnontieteellinen tiedekunta

Computer Organization II

- Advanced (master) level course!
- Prerequisite: Computer Organization I (TiTo)
  - Main hardware
  - Symbolic assembly language, machine instructions
  - Instruction cycle (on CPU)
- Related to Operating Systems
  - Interrupts
  - Virtual memory
  - I/O Techniques

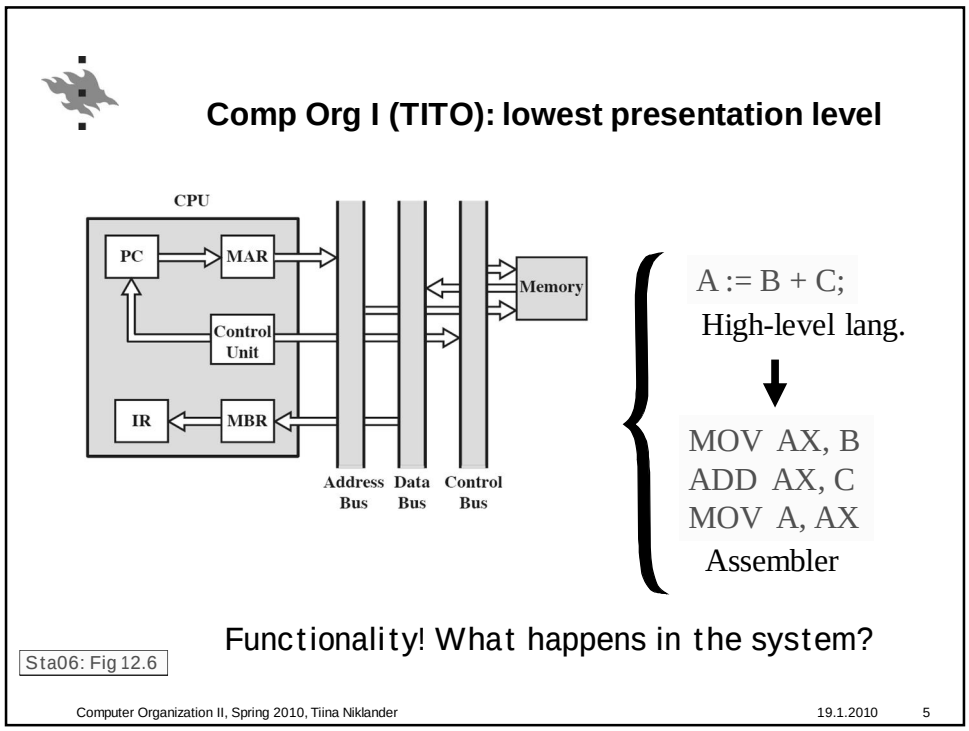
Material

- Course book (Make sure you have one!)
  - Stallings W.: Computer Organization & Architecture, Designing for Performance (8th ed), Prentice-Hall, 2009.
  - (7&6th ed.) possible, but MISSING a lot of material
- Course page (for this Spring course) http://www.cs.helsinki.fi/u/niklande/opetus/tikra/2010/index.en.html
  - Slides, exercises, announcements, links, etc.
- Course main page http://www.cs.helsinki.fi/kurssit/syventavat/581365/
  - Old courses, slides in Finnish and English, etc.
- Newsgroup: hy.tktl.opiskelu.tikra

Schedule Spring 2010

- Lectures: 18.1. – 26.2.2009
  - In Finnish: Tue and Thu 14-16, D122
  - English summary: Fri 12-14 CK111 (Mon 18.1. 14-16 C220)
- Exercises:
  - In English: Päivi Kuuppelomäki Wed 14-16 CK111
  - In Finnish: Tiina Niklander Wed 16-18 C222
- Course Exam
  - Wed 3.3. 16.00-19 A111

- Separate exams are also available


Comp Org I (TITO): lowest presentation level
CPU
PC
MAR
Control Unit
IR
MBR
Memory
Address Bus
Data Bus
Control Bus
A := B + C;
High-level lang.
MOV AX, B
ADD AX, C
MOV A, AX
Assembler
Functionality! What happens in the system?
Sta06: Fig 12.6
Computer Organization II, Spring 2010, Tiina Niklander
19.1.2010
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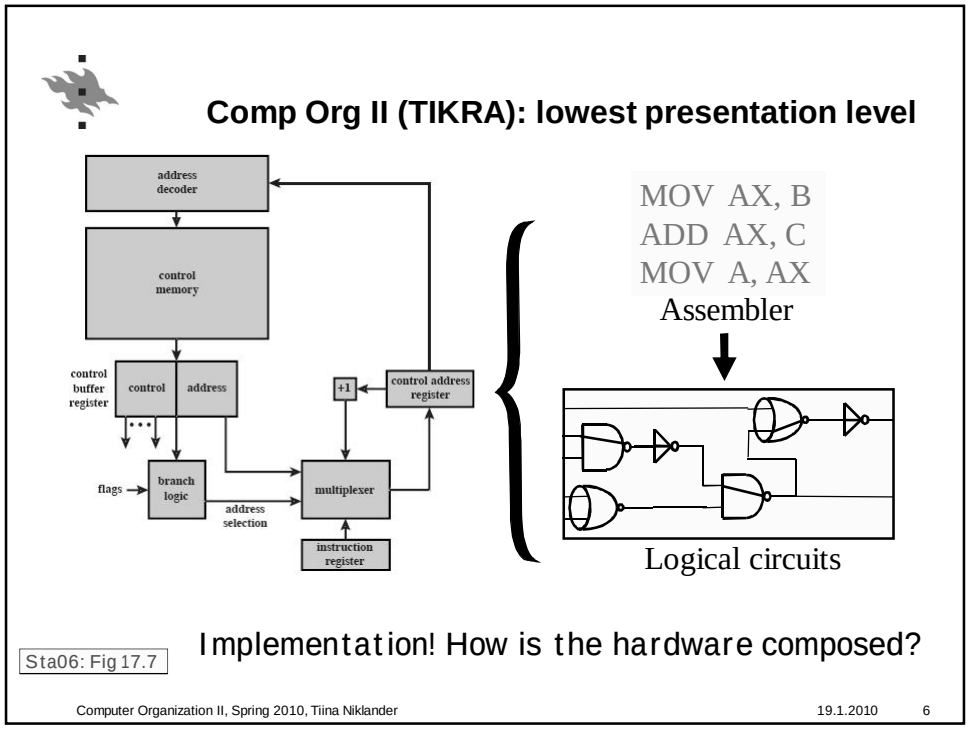
Comp Org II (TIKRA): lowest presentation level
address decoder
control memory
control buffer register
control
address
+1
control address register
flags
branch logic
address selection
multiplexer
instruction register
MOV AX, B
ADD AX, C
MOV A, AX
Assembler
Logical circuits
Implementation! How is the hardware composed?
Sta06: Fig 17.7
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Learning goals

- **Digital logic:** truth table, flip-flop, ...
- **Bus:** multiplexing, signaling
- **Memory hierarchy:** cache, TLB
- **Arithmetics**: Booth algorithm, representations
- **Instruction set**: operands, operations, memory reference
- **Processor structure and functions**: pipelining, RISC,CISC
- **Control**: micro-operations, micro-programmed control, clock pulse
- **Parallel Processing:** cache coherence, multicore

More detailed learning goals (at the moment only in Finnish) are available from course main page

Course content and schedule

- Week 1
  - Overview (Ch 1 – 8)
  - Bus (Ch 3)
  - Self-study: Digital logic
- Week 2
  - Memory, cache (Ch 4, 5)
  - Virtual memory(Ch 8.3-8.6)
- Week 3
  - Computer arithmetics (Ch 9)
  - Instruction set (Ch 10, 11)
- Week 4
  - CPU struc.& func. (Ch 12)
  - RISC-architecture (Ch 13)
- Week 5
  - Instruction-level parallelism, superscalar processor (Ch 14)
  - Control Unit (Ch 15-16)
- Week 6
  - Parallel Processing & Multicore (Ch 17-18)
  - Recapitulation

Motto

”It is not good exercise,
If you do not sweat”

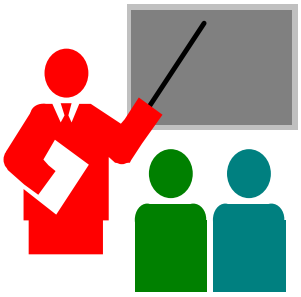
“Kunto ei nouse
ellei tule hiki.”

Work during the course

- Combine the details together to form a larger picture (in your mind)!
  - Try to continuously understand and analyse the connections
  - Stay awake!
- **Make notes**
  - Write down own ideas and questions immediately
- **Ask questions**
  - Question are never too simple. (If you missed the point, then somebody else missed it also)
  - Ask from teachers but *also from co-students.*
- **Teamwork is allowed** even with individual assignments
  - However, own paper must be written by you, even if you co-operated in learning the content

Be active!

- Do all exercises in advance!
  - On your own / in small teams.
  - Think about the problem during several days
    - at least before giving up
  - **Learning by doing!**
- Ask about the problematic parts
  - During lectures
  - While solving the questions
  - When solutions are presented
  - Afterwards from instructors
  - Beginning of next meeting



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Note!

- These slides are just the “table of content”
  - ~ notes of the lecturer
- **Read the book!**
  - ~ just following the lectures or summary is not enough
- Spend enough time in learning the content
  - Simple time estimation (for planning)
  - VERY OLD: ~ 6,5 weeks*(2*(4+2)) = 78 hours
  - OLD: 4 op = 2 ov: 2 * 40 = 80 hours
  - CURRENT: 1 year / 60 op = 1600 t / 60 op
    = 26.67 t / 1 op = 107 hours / 4 op

Enjoy the course!

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Credits

- Teemu Kerola 1999-2003
  - Original slides (in English), blue layout
    - Based on 5th edition
  - Updated to 6th edition 2002
- Auvo Häkkinen 2004-2005
  - Most slides translated to Finnish, orange layout
    - Figures integrated to slides
  - Updated to 7th edition 2005
- Teemu Kerola 2006
- Liisa Marttinen 2007
- Tiina Niklander
  - 2009: Translation to English from the Finnish slide set
  - 2010: Updated to 8th edition