

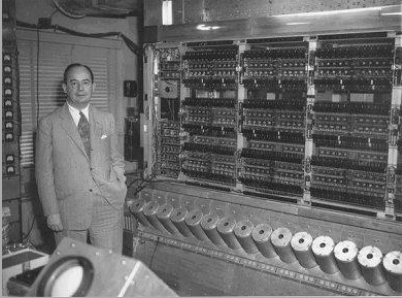
■ HELSINGIN YLIOPISTO
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Lecture 1

Computer systems-overview

Ch 1 - Ch 8 [Sta06]
Some material from
Comp. Org I

John von Neumann
and EDVAC, 1949



■

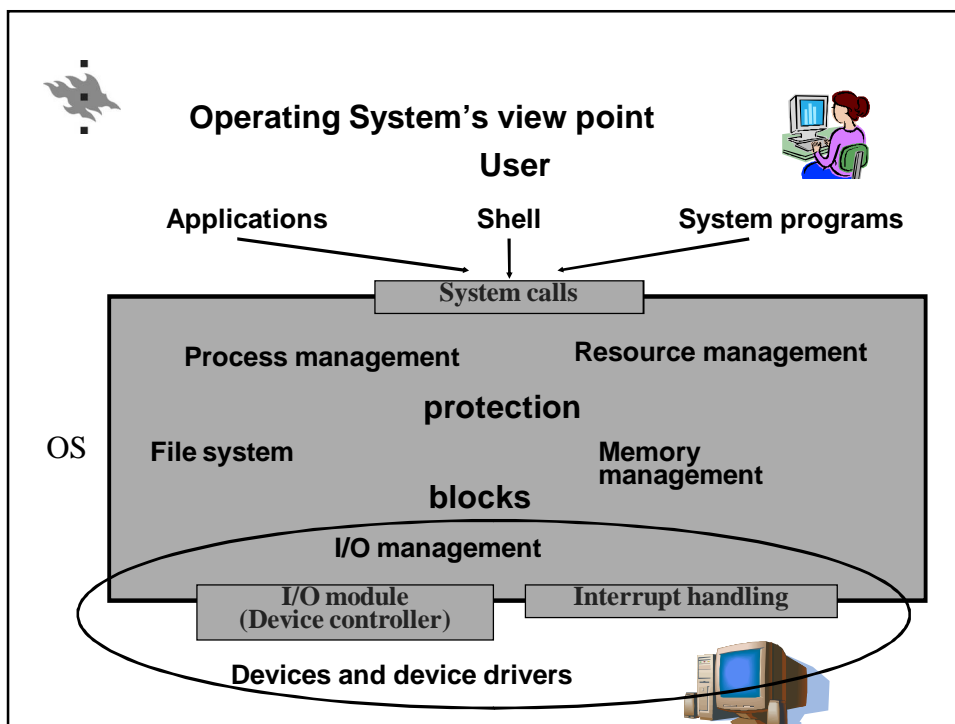
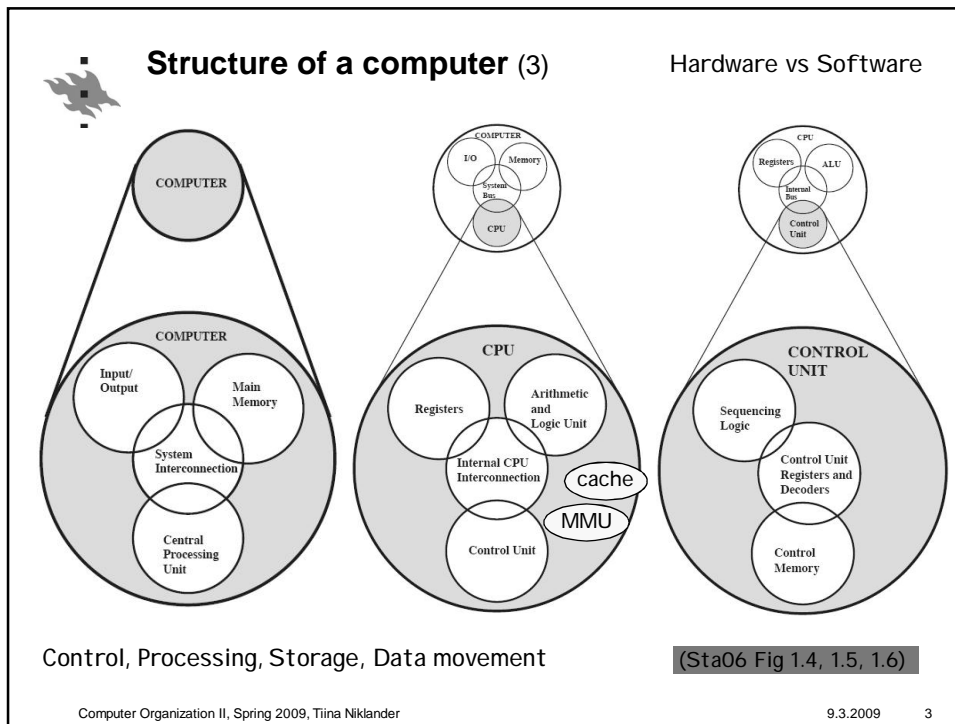
Content

- Structure
- OS view point
- Buses
- I/O-controller and memory-mapped I/O
- Memory hierarchy
- I/O layers
- Privileged mode
- Instruction cycle
- Interrupt handling

■ Goal:

- Remind what has already been covered on Comp. Org I

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Buses

- Local (*Sisäinen*), System, I/O expansion
- Device controllers (*Laitteohjaimet*), NOTE: Sta06: I/O module

(a) Traditional Bus Architecture (Sta06 Fig 3.18 a)

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I/O controller and memory-mapped I/O

(Sta06 Fig 7.3)

- Device driver (*ajuri*) controls the device via controller's registers
- Driver refers to these registers as regular memory locations
 - Common memory references, like in load/store -instructions
 - Controller (*ohjain*) detects its own memory addresses on the bus
 - Device controller ~ 'intelligent' memory location

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Memory hierarchy

Typical access time		Typical capacity
1 nsec	Registers	<1 KB
2 nsec	Cache	4 MB
10 nsec	Main memory	512-2048 MB
10 msec	Magnetic disk	200-1000 GB
100 sec	Magnetic tape	400-800 GB

Figure 1-9. A typical memory hierarchy. The numbers are very rough approximations.

- Access time (*saantiaika*) (un?)dependent of the location
 - Registers, cache, main memory
 - Block buffering (*lohkopuskurointi*) (OS functionality!)
 - Magnetic and optical storage devices
- File servers (*tiedostopalvelimet*)
 - Network Attached Storage (NAS)
 - Storage Area Network (SAN)

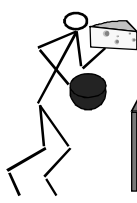
Tan08 Fig 1.9

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Teemu's cheese cake

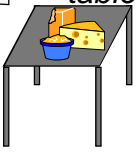
■ Register, on-chip cache, memory, disk, and tape speeds relative to times locating cheese for the cheese cake you are baking...

hand




0.5 sec
(register)

table




1 sec
(cache)

refridge-rator



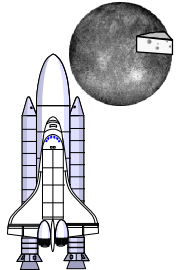
10 sec
(memory)

moon




12 days
(disk)

Europa (Jupiter)



4 years
(tape)

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The diagram shows two ovals labeled 'user' and 'kernel' connected by two curved arrows pointing in opposite directions, representing the transition between execution modes.

CPU execution modes

- Instruction privileges
 - Privileged (*etuoikeudet*) and normal
- Memory protection
 - Memory area marked for a user and controlled access
- User mode (*käyttäjätila*)
 - May use only normal instructions
 - Can refer only to its own memory area
- Kernel mode (*etuoikeutettu tila*)
 - Can use all instructions, including the privileges ones
 - May refer to all memory locations, including the kernel data structures of the operating system

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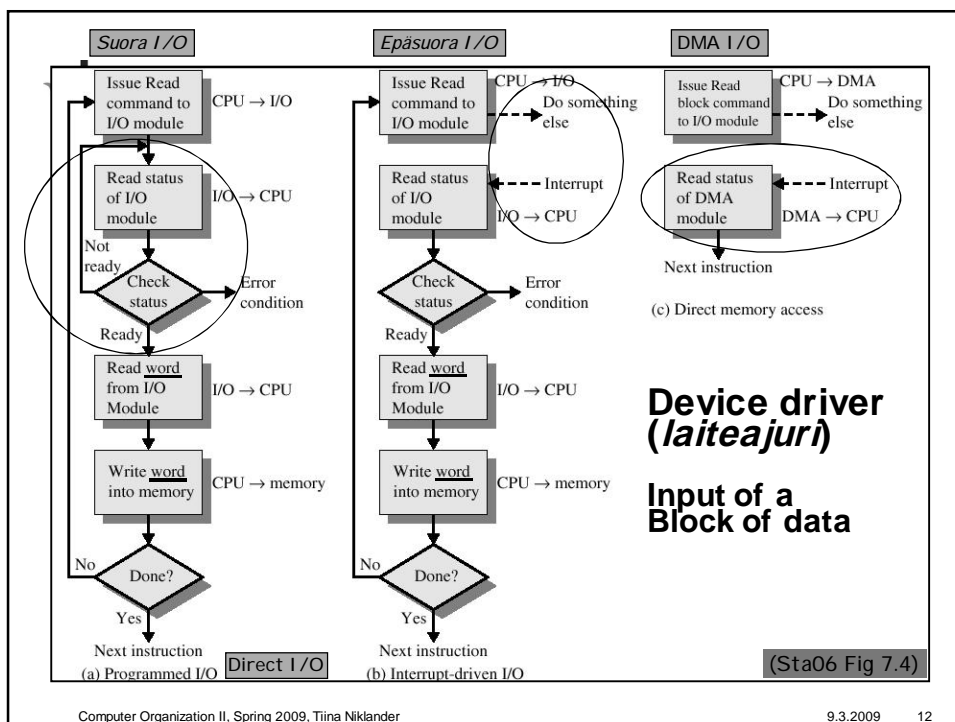
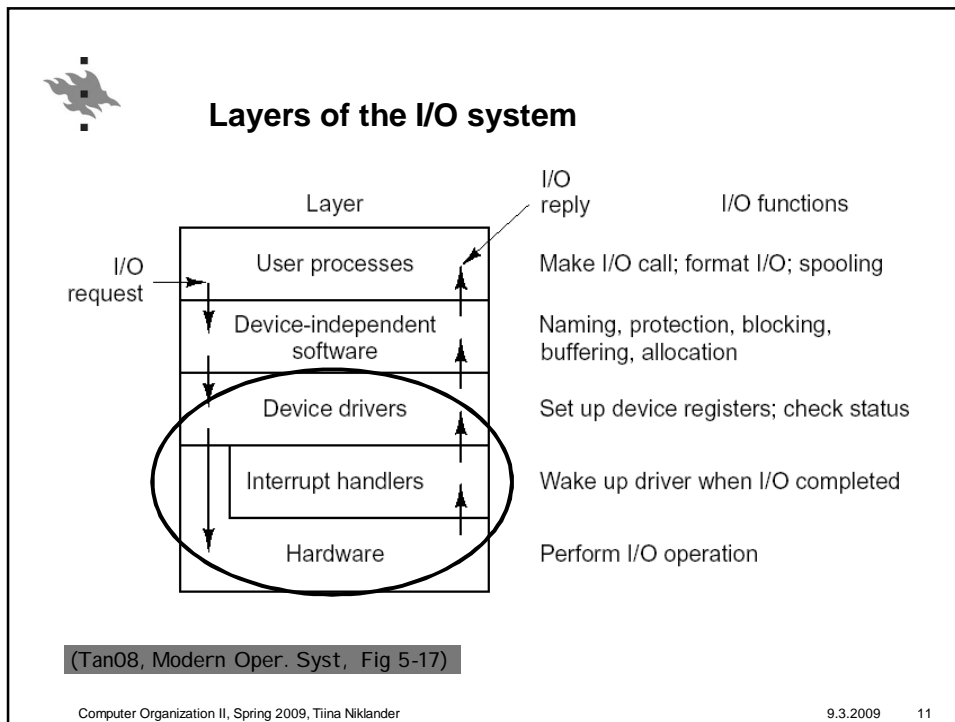


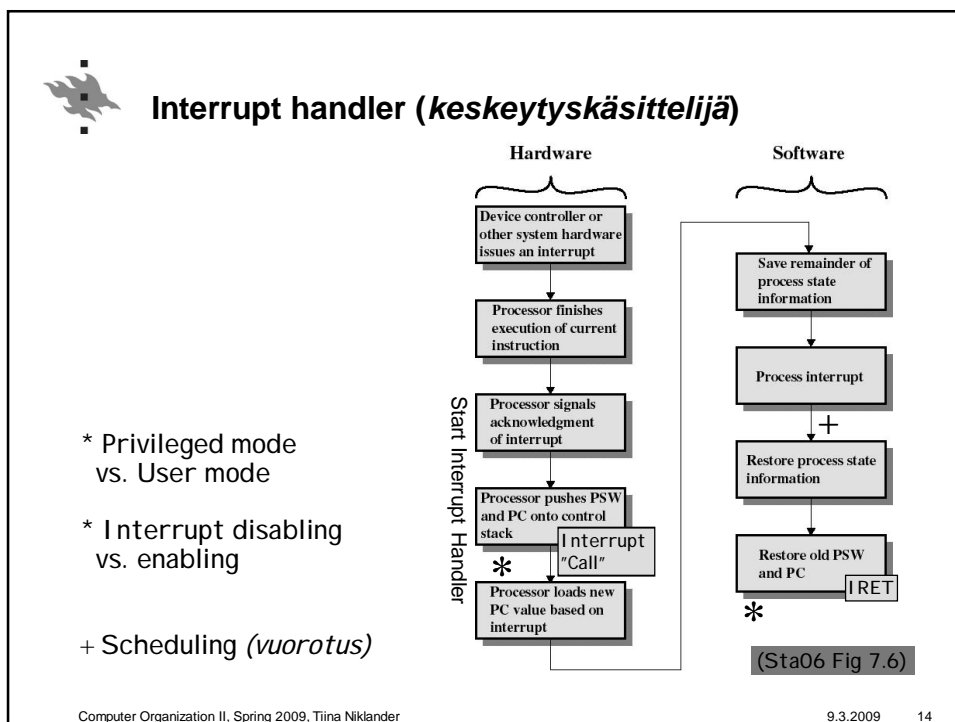
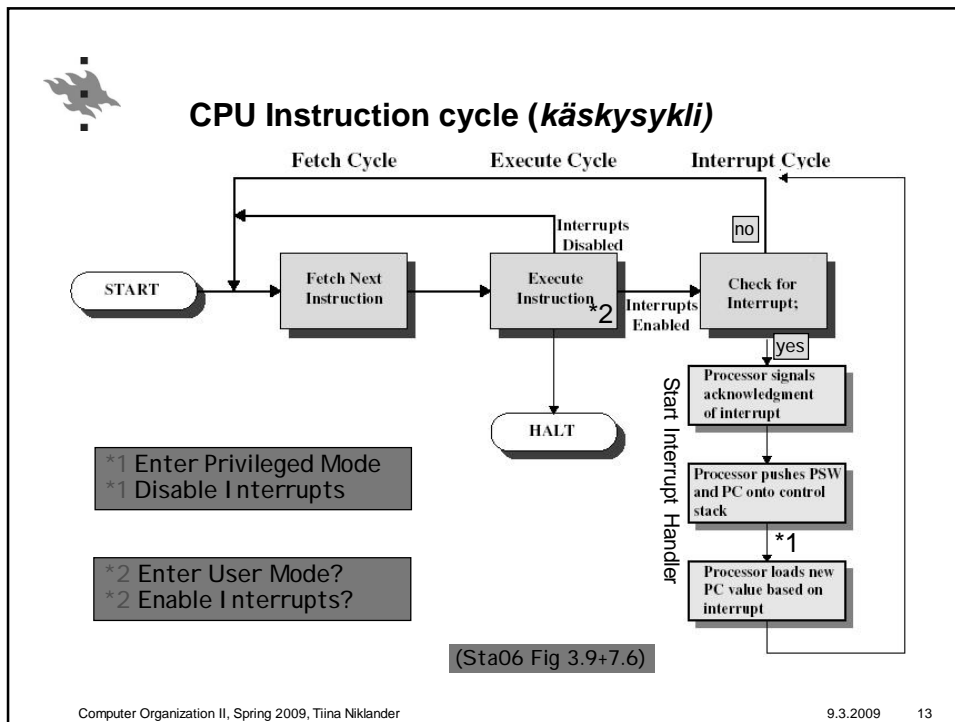
The diagram shows two ovals labeled 'user' and 'kernel' connected by two curved arrows. The top arrow points from 'user' to 'kernel' and is labeled 'SVC, INT'. The bottom arrow points from 'kernel' to 'user' and is labeled 'IRET'.

Mode change

- User mode, normal mode → kernel mode, privileged mode
 - Interrupt or special SVC instructions (service request)
 - Interrupt handler checks the right for mode change
- Kernel mode → User mode
 - Privileged instruction, for example IRET (return from interrupt)
 - Returns the control and mode as they were before the mode change
 - Very similar with return from a subroutine

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Review Questions

- Course book: at the end of each chapter
 - Answers in the chapter text
- From earlier courses: (see web)
 - Mainly in Finnish, created in project in earlier courses
- Create yourself:
 - List the most difficult and/or important issues
- Think at least about these:
 - Main parts of a computing system?
 - DMA: principles and functionalities?
 - Obligatory hardware and its features?
 - How to make CPU to execute normal user program?
Operating system?